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(71) Applicant
Varian Associates Inc (USA-Delaware),
611 Hansen Way, Palo Alto, California 94303, United States of America

(72) Inventors
Armand P. Neukermans,
Graham J. Siddall,
Joseph W. Franklin

(74) Agent and/or Address for Service
Stanley Popplewell Poole,
57 Lincoln's Inn Fields, London WC2A 3LS

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US 3652075
GB 1334583

(58) Field of search
B3D

(54) Chuck

(57) A vacuum chuck 1 for holding a semiconductor wafer during photolithographic processing is fabricated from a single piece of monolithic silicon. Flat peaks 11 support the wafer and valleys 13 provide air flow paths so that a vacuum source 17 may be used to draw the wafer down onto the chuck. A high voltage may be applied to the chuck to cause an electrostatic force across a dielectric layer to draw a grounded wafer onto the chuck.

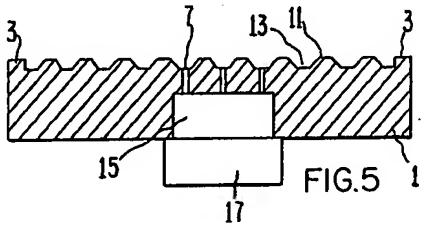

FIG.5

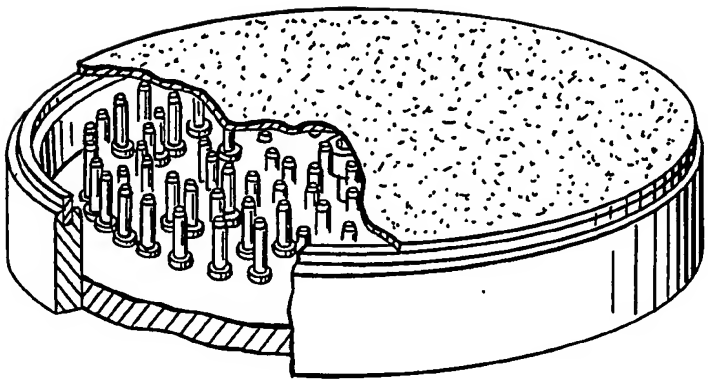

FIG. 1 (PRIOR ART)

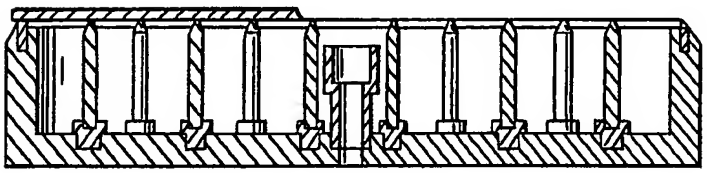

FIG. 2 (PRIOR ART)

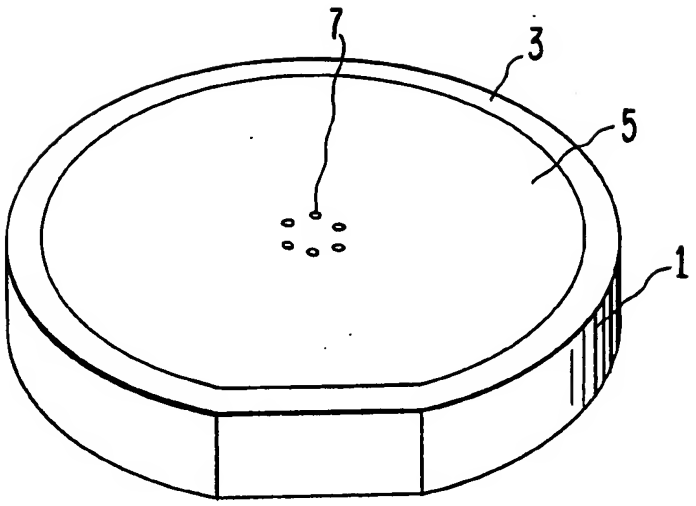

FIG.3

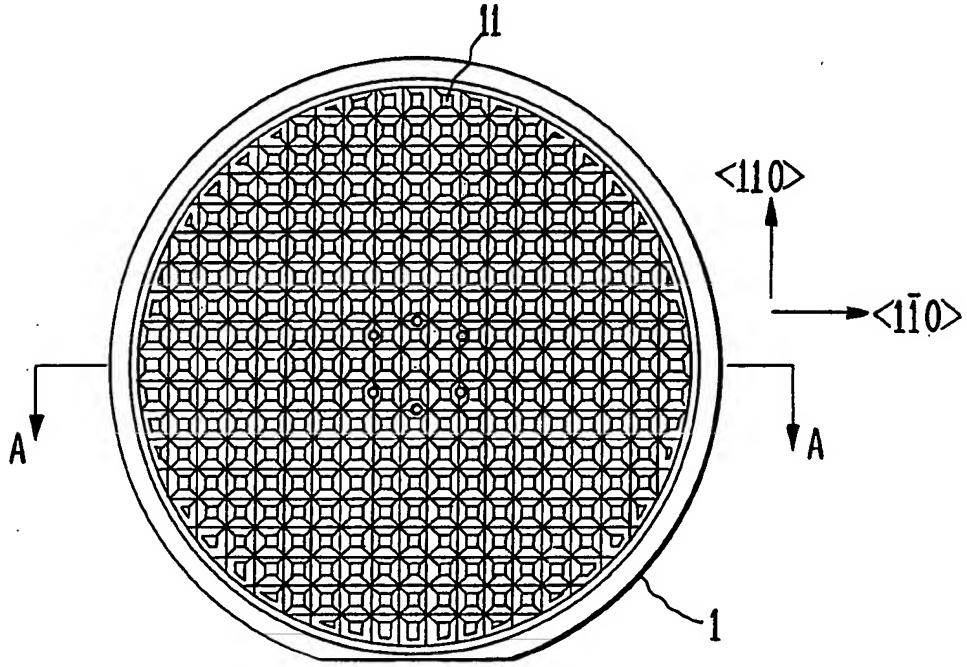

FIG.4

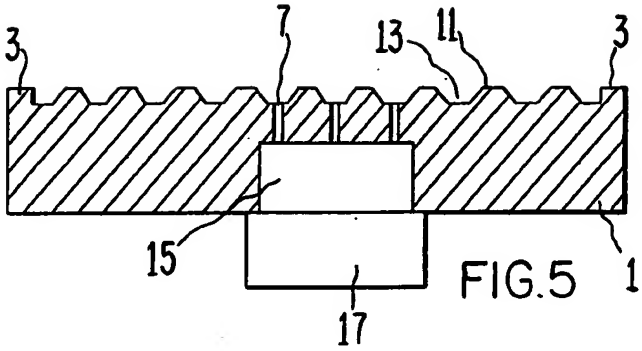

FIG.5

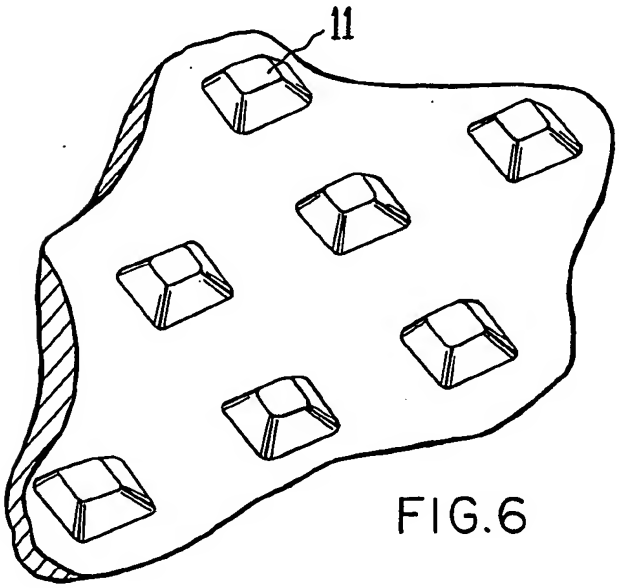

FIG.6

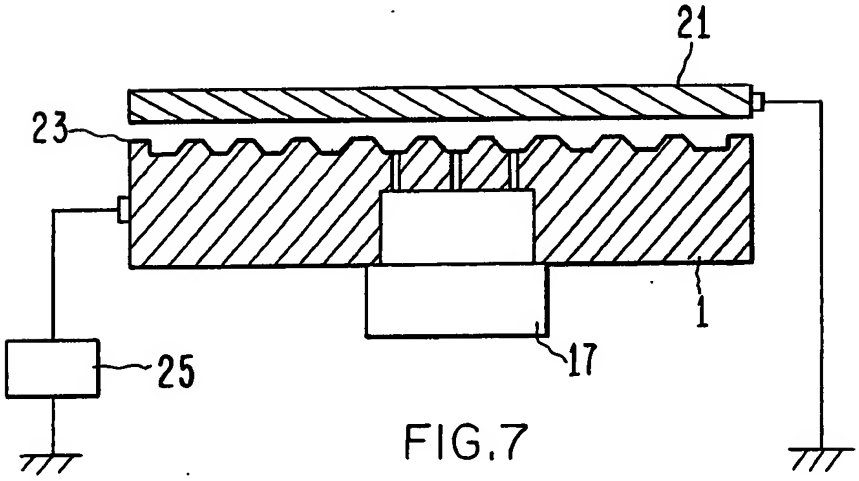

FIG.7

SPECIFICATION

Pin chuck

During photolithographic processing, a semi-conductor wafer is securely mounted to a chuck for accurate positioning. For optimal results, it is important that the wafer be securely attached to the chuck and that the chuck present a flat mounting surface to the wafer.

A typical prior art pin chuck is disclosed in U.S. Patent No. 4,213,698. As shown in Figures 1 and 2 herein, such a prior art chuck utilizes a vacuum source to draw a wafer down onto a number of metal support posts. Such prior art chucks are expensive to fabricate and the wafer may be strained and distorted since the metal chuck and the semiconductor wafer have different coefficients of thermal expansion. Further, because the wafer mounting surface is metal, cold welding and subsequent diffusion chamber contamination may occur.

According to the invention there is provided a workpiece mounting device, as set out in claim 1 of the claims of this specification. In one example, a vacuum pin chuck is fabricated from a single piece of monolithic silicon. The surface of the chuck is polished flat and etched so that an annular outer sealing surface surrounds an interior region of flat peaks and valleys. Holes drilled through the interior region allow for the application of a vacuum. Contact to a semiconductor wafer to be processed is made only at the annular surface and at the peaks of the interior region. Air flow paths through the valleys allow the vacuum to draw the wafer securely onto the flat peaks and the annular sealing surface. Since the area of the mounting surface (composed of the annular sealing surface and the tops of the peaks) is approximately only four percent of the pin chuck surface area the probability is low that a piece of grit would come between the wafer and the mounting surface. And, since the chuck and the wafer may be fabricated from the same material, the coefficients of thermal expansion of the wafer and the chuck are the same. Further, cold welding between the chuck and the wafer does not affect chuck flatness since a broken peak fractures without burring. In addition, cold welding of the chuck to the wafer cannot cause contamination of a diffusion chamber used in a later processing step since the chuck material is inert.

In an alternative preferred embodiment of the present invention, an electrostatic force is used to securely draw the wafer to the chuck. A dielectric material is applied to the wafer mounting surface, the wafer is grounded and a high voltage is applied to the pin chuck. The vacuum source may be used initially to draw the wafer into contact with the chuck and the electrostatic force serves to securely hold the wafer to the chuck once the distance between the wafer and the chuck is small.

Figure 1 shows a perspective view of a prior art pin chuck.

Figure 2 shows a side view of the pin chuck shown in Figure 1.

Figure 3 shows a perspective view of a pin chuck which is constructed in accordance with the preferred embodiment of the present invention.

Figure 4 shows a top view of the chuck shown in Figure 3.

Figure 5 shows a side view, along line A-A, of the chuck shown in Figure 4.

Figure 6 shows a magnified view of the interior region of the chuck shown in Figure 3.

Figure 7 shows an alternative preferred embodiment of the present invention in which an electrostatic force is used to securely hold a wafer to the pin chuck shown in Figure 5.

Figures 1 and 2 show perspective and side views of a typical prior art pin chuck in which discrete posts, usually metal, are used to support the wafer being processed.

Figure 3 shows a perspective view of a monolithic vacuum pin chuck 1 which is constructed in accordance with the illustrated preferred embodiment of the present invention. Chuck 1 comprises a single piece of monolithic silicon which is 3 inches in diameter and .5 inch thick. It is also possible to fabricate chuck 1 from other crystalline materials such as GaAs, quartz or sapphire and to use other chuck dimensions depending upon the size of the wafer to be held by chuck 1. A flat annular sealing surface 3 lies along the outer edge of the upper surface of chuck 1 surrounding an interior region 5. Six through air holes 7 are drilled through chuck 1 to allow connection to a vacuum source.

Figure 4 shows a top view of chuck 1 and Figure 5 shows a side view along line A-A; interior region 5 is shown out of scale in both drawings to emphasise peaks 11 and valleys 13. For a typical three inch diameter chuck 1 as discussed above, the annular sealing surface 3 is 5 millimeters wide, the flat tops of peaks 11 are 200 microns, the centers of peaks 11 are spaced approximately 1000 microns apart and the flat tops of peaks 11 are 50 microns above the floor of valley 13. Holes 7 are .03 inch in diameter and a manifold 15 may be milled into the underside of chuck 1 to facilitate the attachment of a vacuum source 17. Various chucks 1 have been constructed in which the height of peaks 11 above valleys 13 has been increased up to 100 microns.

Figure 6 shows a reproduction of a scanning electron micrograph of a portion of interior region 5. In this view, peaks 11 may be seen as flat-topped pyramids although other configurations, e.g. square posts, may be used as desired.

Chuck 1 is fabricated from a single piece of monolithic silicon having a 100 crystalline lattice orientation. Silicon having other crystalline lattice orientations may be used as desired to fabricate peaks 11 having various other geometries. Chuck 1 is initially cut to the desired size and manifold 13 is milled. The upper surface (comprising annular sealing surface 3 and interior region 5) is polished to the desired degree of flatness which may be to a submicron level using well known modern techniques. A stress relieving layer of oxide is depos-

ited on the upper surface and a nitride mask, patterned to allow the desired etching of peaks 11 and valleys 13, is deposited over the stress relieving oxide layer. An orientation dependent etchant (such as KOH for the 100 silicon described above) is then used to etch peaks 11 and valleys 13. Finally, the nitride mask is removed and a wear layer of nitride is deposited over the stress relieving oxide layer.

In use, a wafer having a diameter which is approximately the same as the diameter of chuck 1 is placed upon the upper surface of chuck 1. Flat annular sealing surface 3 provides an air seal around the edge of the wafer. A vacuum applied by vacuum source 17 through manifold 13 and holes 7 draws the wafer down onto annular surface 3 and peaks 11. The many peaks 11 provide a large number of flat support points for the wafer.

Figure 7 shows an alternative preferred embodiment of the present invention in which both vacuum and electrostatic forces are used to draw a wafer 21 onto the pin chuck 1 shown in Figure 5. A dielectric layer 23 is deposited over the peaks 11 and valleys 13 of the pin chuck 1. Dielectric layer 23 may comprise, for example, a 2-3 micron thick layer of silicon dioxide. A high voltage on the order of 1000 volts is applied to chuck 1 by a supply 25 and the wafer 21 is grounded. In operation, the vacuum source 17 is used first to draw wafer 21 close to chuck 1. Then supply 25 is energized and an electrostatic force proportional to the square of the supply 25 voltage (and inversely proportional to the square of the distance between chuck 1 and wafer 21) is exerted to draw the wafer 21 onto the peaks 11 of chuck 1. The area of peaks 11 may be increased relative to the area of the upper surface in order to increase the electrostatic force and in such a case the vacuum source 17 and annular sealing ring 3 migh not be needed.

CLAIMS

1. A mounting device for supporting a workpiece, comprising:
a chuck having a plurality of peaks for supporting the workpiece; and
wherein the chuck is composed of a single piece of crystalline matter.

2. A mounting device as in claim 1, wherein the peaks are formed by etching the single piece of crystalline matter.

3. A mounting device as in claim 2, wherein the peaks have tops which are substantially flat.

4. A mounting device as in claim 3, wherein the peak tops are substantially coplanar.

5. A mounting device as in claim 4, wherein the peaks are substantially flat-topped pyramids.

6. A mounting device as in claim 4, further comprising an annular sealing surface which is substantially flat and coplanar with the tops of the peaks.

7. A mounting device as in claim 6, further comprising:
valleys defined by the peaks;
a manifold for receiving a vacuum; and
one or more holes in the chuck, said holes connecting the manifold to one or more of the valleys.

8. A mounting device as in claim 1, wherein the crystalline matter is silicon.

9. A mounting device as in claim 8, wherein the silicon has 100 crystalline lattice orientation.

10. A mounting device as claimed in claim 7, further comprising a vacuum source connected to the manifold.

11. A mounting device as claimed in claim 7, or any claim dependent thereon, further comprising:
a dielectric layer overlaying the peaks; and
a high voltage supply coupled to the chuck.

12. A workpiece mounting device substantially as herein described with reference to and as illustrated in Figures 3 to 6 alone or as modified by Figure 7 of the accompanying drawings.

13. A mounting device as in any one of the preceding claims in combination with a workpiece, wherein the workpiece comprises the crystalline matter.

14. The combination as in claim 13, wherein the workpiece comprises a semiconductor wafer.

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